Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. **(Currently Amended)** A method for the compensation of interference in a signal generated by discrete multitone modulation, the interference essentially being caused by the transient process of a transmission channel via which the signal is transmitted, the signal having a multiplicity of symbols with digitized samples and each symbol being preceded by a cyclic prefix with digitized samples, having the following steps:

feeding of the digitized samples of the signal to a serial/parallel converter (15);

subtraction of at least one digitized sample of a symbol from a digitized sample [[-]] assigned thereto [[-]] of the cyclic prefix preceding the symbol by means of at least one subtractor circuit (16) for determining interference;

calculation of the transient process of the transmission channel from the determined interference by means of multiplier circuits (17, 18); and

subtraction of the calculated transient process from the digitized samples of the symbol.

2. **(Original)** The method as claimed in claim **1**, characterized in that provision is made of corresponding devices (4, 8; 5, 10; 7, 12) for compensation of the interference both in the time domain and in the frequency domain.

3. **(Currently Amended)** The method as claimed in [~~either of claims 1 and 2~~] claim 1, characterized in that coefficients which are calculated from the error-corrected digitized samples are fed to a system analysis unit (6) from which the properties of the transmission channel are calculated.

4. **(Original)** A circuit arrangement for carrying out the method as claimed in claim 1 [~~one of claims 1 to 3, having~~] the circuit arrangement comprising:

a serial/parallel converter (15), to which the digitized samples of the signal can be fed;

at least one subtractor circuit (16), each subtractor circuit (16) subtracting a digitized sample of the symbol from a digitized sample - assigned thereto - of the cyclic prefix preceding the symbol for a calculation of the error on account of the transient process;

at least one multiplier circuit (17, 18) for multiplication of the error by a specific parameter, at least one multiplier circuit (17, 18) being assigned to each digitized sample of a symbol;

it being possible for the output signal of each subtractor circuit (16) to be fed in each case to each multiplier circuit (17, 18); and

it being possible for the output signal of each multiplier circuit (17, 18) to be subtracted from the corresponding digitized sample of the symbol by means of subtractor devices (19, 20).

5. **(New)** The method as claimed in claim **2**, characterized in that coefficients which are calculated from the error-corrected digitized samples are fed to a system analysis unit (6) from which the properties of the transmission channel are calculated.

6. **(New)** A circuit arrangement for carrying out the method as claimed in claim **2**, the circuit arrangement comprising:

a serial/parallel converter (15), to which the digitized samples of the signal can be fed;

at least one subtractor circuit (16), each subtractor circuit (16) subtracting a digitized sample of the symbol from a digitized sample - assigned thereto - of the cyclic prefix preceding the symbol for a calculation of the error on account of the transient process;

at least one multiplier circuit (17, 18) for multiplication of the error by a specific parameter, at least one multiplier circuit (17, 18) being assigned to each digitized sample of a symbol;

it being possible for the output signal of each subtractor circuit (16) to be fed in each case to each multiplier circuit (17, 18); and

it being possible for the output signal of each multiplier circuit (17, 18) to be subtracted from the corresponding digitized sample of the symbol by means of subtractor devices (19, 20).

7. **(New)** A circuit arrangement for carrying out the method as claimed in claim **3**, the circuit arrangement comprising:

a serial/parallel converter (15), to which the digitized samples of the signal can be fed;

at least one subtractor circuit (16), each subtractor circuit (16) subtracting a digitized sample of the symbol from a digitized sample - assigned thereto - of the cyclic prefix preceding the symbol for a calculation of the error on account of the transient process;

at least one multiplier circuit (17, 18) for multiplication of the error by a specific parameter, at least one multiplier circuit (17, 18) being assigned to each digitized sample of a symbol;

it being possible for the output signal of each subtractor circuit (16) to be fed in each case to each multiplier circuit (17, 18); and

it being possible for the output signal of each multiplier circuit (17, 18) to be subtracted from the corresponding digitized sample of the symbol by means of subtractor devices (19, 20).

8. **(New)** A circuit arrangement for carrying out the method as claimed in claim **5**, the circuit arrangement comprising:

a serial/parallel converter (15), to which the digitized samples of the signal can be fed;

at least one subtractor circuit (16), each subtractor circuit (16) subtracting a digitized sample of the symbol from a digitized sample - assigned thereto - of the cyclic prefix preceding the symbol for a calculation of the error on account of the transient process;

at least one multiplier circuit (17, 18) for multiplication of the error by a specific parameter, at least one multiplier circuit (17, 18) being assigned to each digitized sample of a symbol;

it being possible for the output signal of each subtractor circuit (16) to be fed in each case to each multiplier circuit (17, 18); and

it being possible for the output signal of each multiplier circuit (17, 18) to be subtracted from the corresponding digitized sample of the symbol by means of subtractor devices (19, 20).